

Fig 1

<u>Inst</u>	<u>Hit/Miss</u>	<u>Data</u>	
18 — LDR [R <sub>n</sub> ]	Hit	Data [R <sub>n</sub> ]	
MOV	N/A	—	
CMP	N/A	—	
⋮	⋮	⋮	
20 — LDR [R <sub>n</sub> ]	Miss	—	<div> <div></div> <div>variable delay</div> <div></div> </div>
MOV	N/A	—	
CMP	N/A	Data [R <sub>n</sub> ]	
⋮			
22 — LDR [R1]	Miss	—	
24 — LDR [R2]	Miss	—	
MOV	N/A	—	
CMP	N/A	28 — Data [R2]	<div> <div>missed data returned out of order</div> </div>
ADD	N/A	26 — Data [R1]	

Fig. 2

Instruction Trace Stream

⋮

30 — LDR[R1] -- miss  
 MOV  
 CMP

34 — LDR[R2] -- hit  
 LDR[R3] -- miss

38 — ADD  
 MOV  
 SUB  
 ⋮

Data Trace Stream

⋮

32 — Data Placeholder Tag 1  
 —  
 —

36 — Data [R2]  
 Data Placeholder Tag 2

40 — —

42 — Late Data Tag 2 [R3]  
 Late Data Tag 1 [R1]  
 ⋮

Fig. 3

Instruction Trace Stream

⋮

46 — LDR[R1] -- miss  
 CMP  
 ADD

50 — LDR[R2] -- hit  
 LDR[R3] -- miss  
 SUB  
 MOV

56 — LDR[R4] -- miss  
 CMP  
 MOV  
 ⋮

Data Trace Stream

⋮

48 — Data Placeholder Operating  
 —  
 —

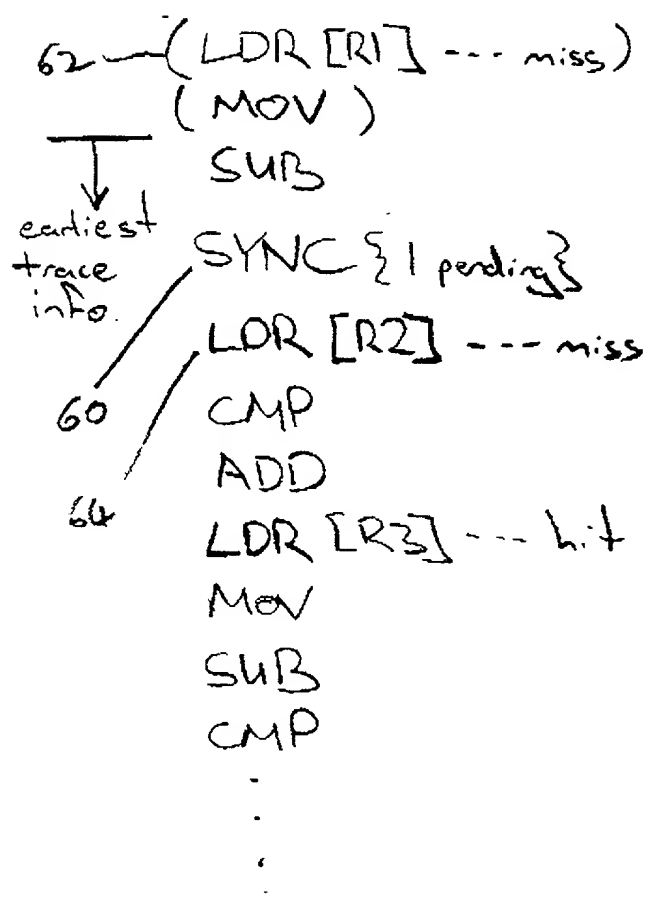
52 — Data [R2]  
 Data Placeholder 1 pending  
 Late Data [R1]

54 — —

58 — Data Placeholder 1 pending  
 Late Data [R3]  
 Late Data [R4]  
 ⋮

Fig. 4

Instruction Trace Stream



Data Trace Stream

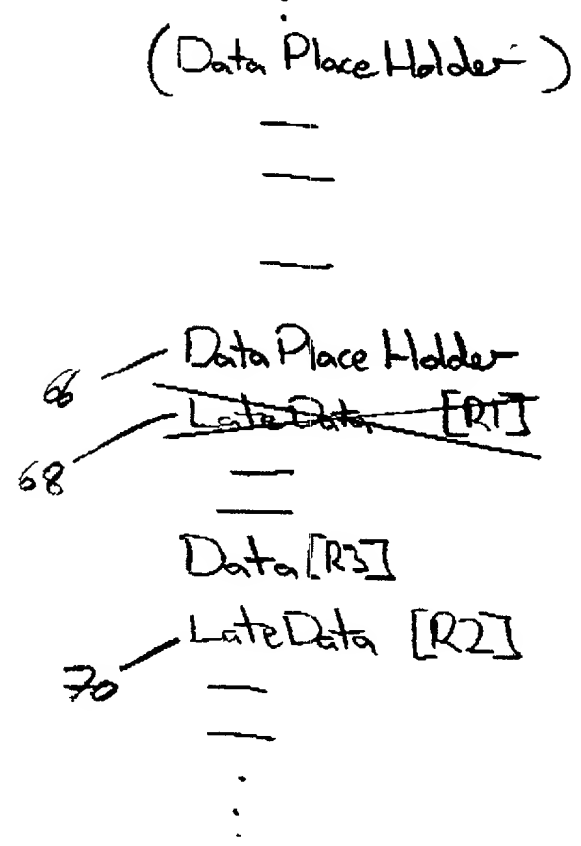


Fig. 5

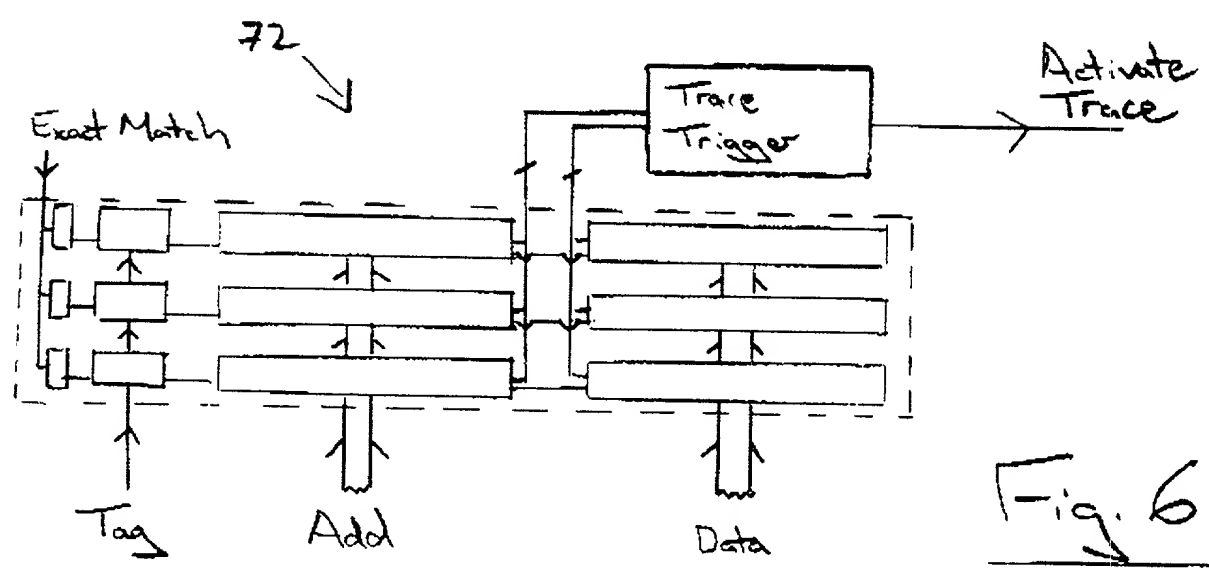


Fig. 6

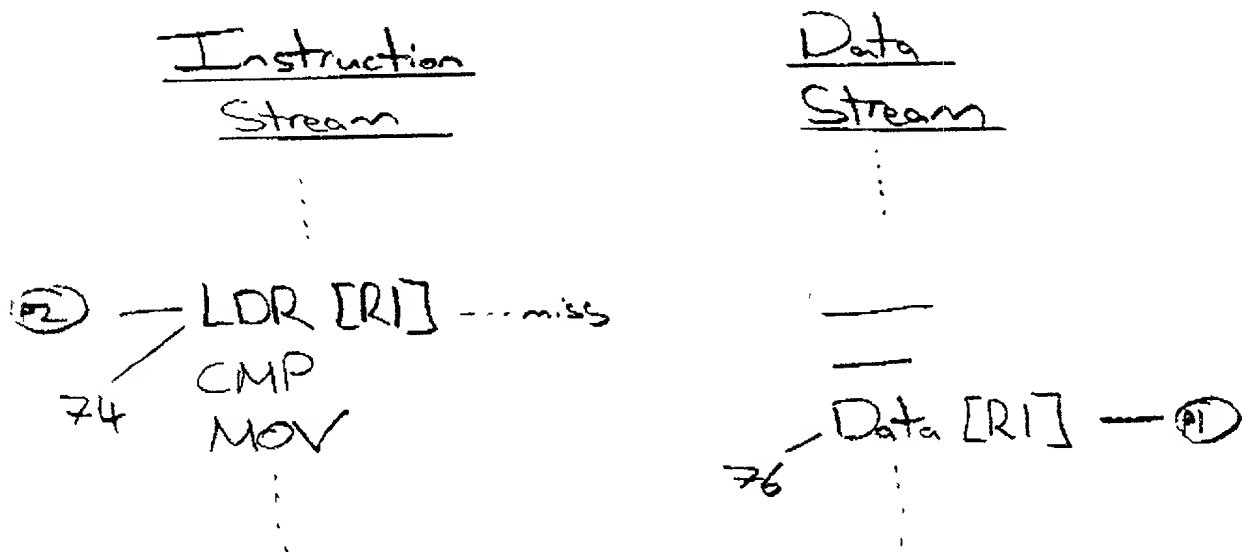


Fig. 7

Exact Match	Add Match	Data Match	Trace Activation Point
✓	✓	✓	①
✓	✓	X	none
X	✓	✓	②
X	✓	X	②

Fig. 8

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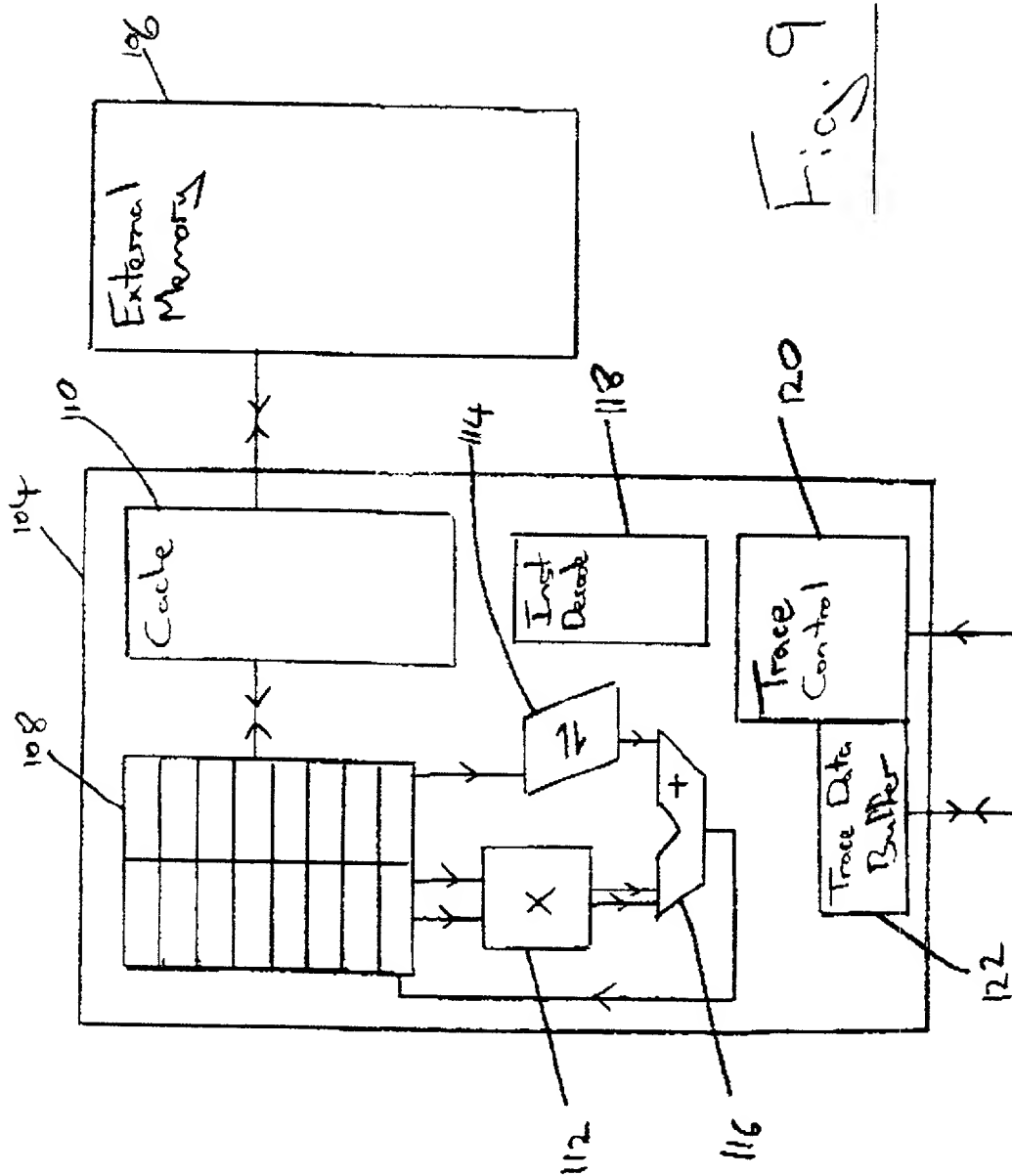


Fig. 9

LSM  $R_n[Add]$ ,  $\underbrace{Reg\ List}_{16\ bits}$

0000 1000 1000 1011



R0	
R1	
R3	R11
R7	

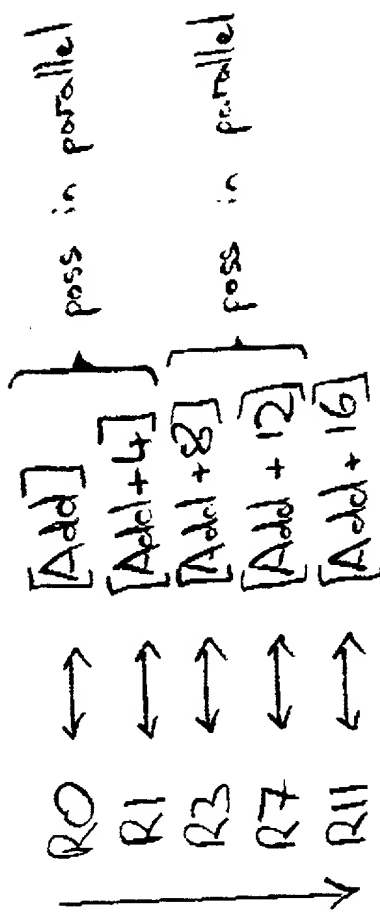


Fig. 10

R0  $\xleftrightarrow{DW_1}$  [Add]

R1  $\xleftrightarrow{DW_2}$  [Add+4]

R3<sup>#</sup>  $\xleftrightarrow{DW_3^*}$  [Add+8]!

R7  $\xleftrightarrow{DW_4}$  [Add+12]

R11  $\xleftrightarrow{DW_5}$  [Add+16]

Trace  
Trigger

Trace  
to  
End



Trace Data Stream

..... {LSNR}, {DW<sub>3</sub>}, {Add+8}, {Place Holder}; {Place Holder};

← Count back to R3

Fig. 11



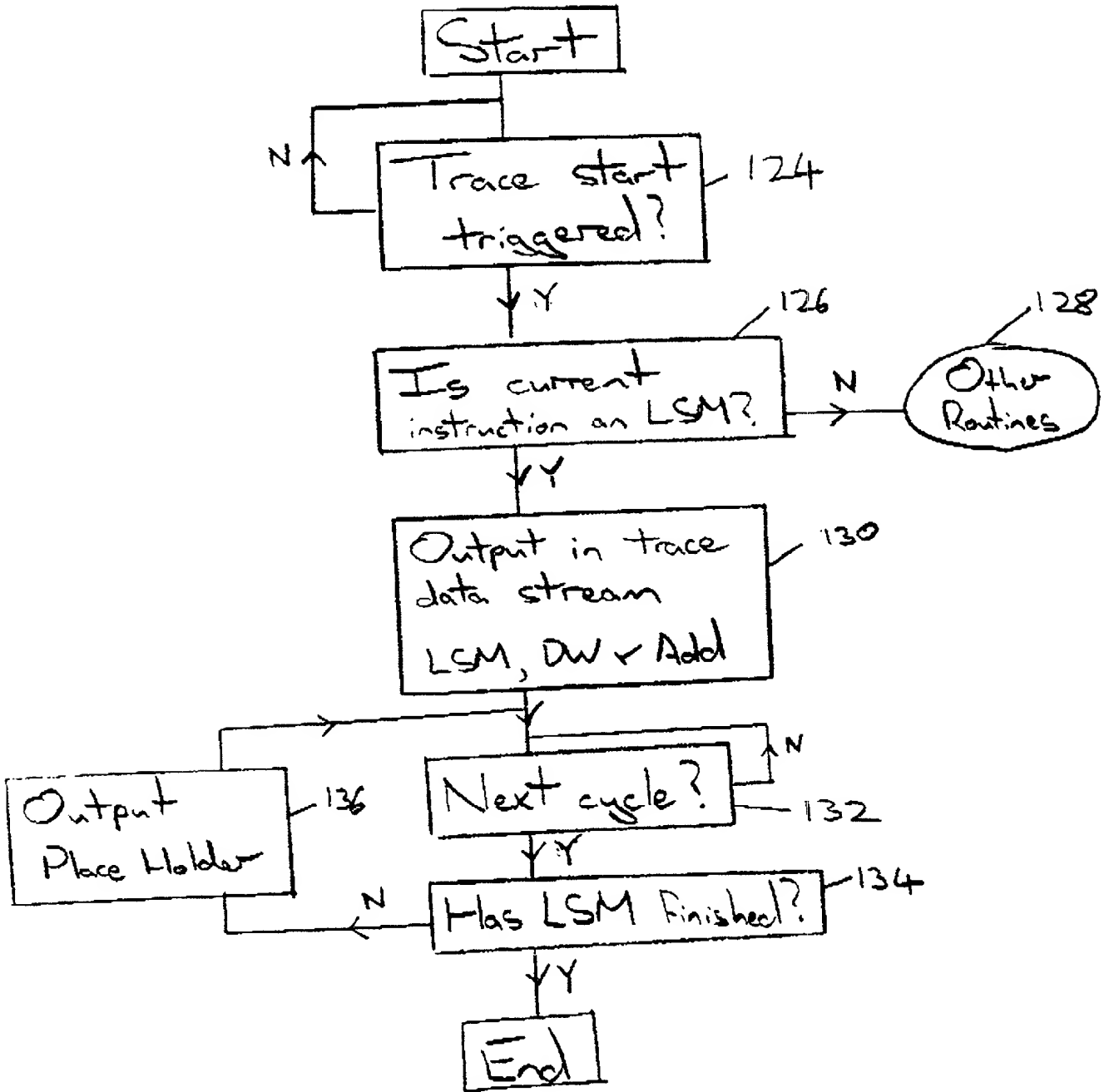


Fig. 12

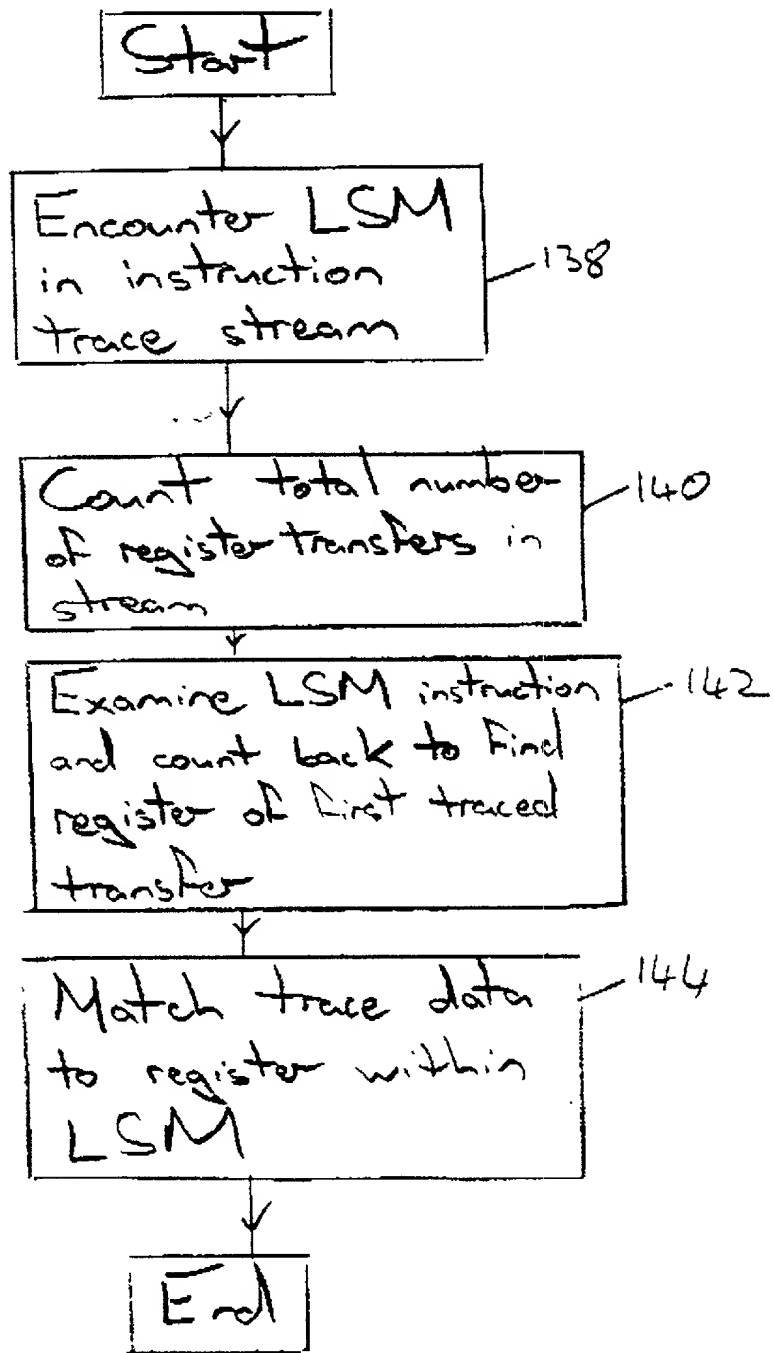


Fig. 13